BGA Fanout and Escape Routing Planning Checklist

Pre-Layout and Pre-Release Engineering Review | Excel Circuit | www.excelcircuit.com

Project / Board:	PCB Revision:	BGA / Processor:	Package / Pitch:
Review Date:	Reviewer:	Target Fabricator / Process:	

Area	Check	Status	Notes
1. Package and Pitch	Confirm the released BGA package, ball count, pitch and pad-field geometry before selecting the fanout strategy.	□ Pass □ Review □ N/A	
2. Ball Map	Review signal, power, ground, NC/reserved and constrained interface pins.	□ Pass □ Review □ N/A	
3. Stackup	Confirm available signal layers, plane references and intended routing-layer strategy.	□ Pass □ Review □ N/A	
4. Via Strategy	Select an appropriate through-via, blind-via, microvia or via-in-pad approach based on density, stackup and fabrication capability.	□ Pass □ Review □ N/A	
5. Escape Channels	Estimate available routing channels and reserve space for the most constrained signal groups.	□ Pass □ Review □ N/A	
6. Escape Direction	Plan route distribution around the package while considering nearby memory, connectors, keepouts and mechanical constraints.	□ Pass □ Review □ N/A	
7. Power / Ground Breakout	Review power and ground escape paths, plane access and local decoupling strategy.	□ Pass □ Review □ N/A	
8. High-Speed Interfaces	Identify DDR, PCIe, clocks, differential pairs or other constrained interfaces that affect breakout planning.	□ Pass □ Review □ N/A	
9. Reference Planes / Return Paths	Review layer transitions and reference-plane continuity through the BGA escape region.	□ Pass □ Review □ N/A	
10. Via-in-Pad Process	Document filling, planarization, plating-over or other via-in-pad requirements where required by design, assembly or fabrication process.	□ Pass □ Review □ N/A	
11. HDI Build Coordination	Confirm microvia layer pairs, sequential-lamination needs and other HDI assumptions with the intended fabrication process where applicable.	□ Pass □ Review □ N/A	
12. Fabricator Capability	Confirm critical geometry and via structures against the selected fabricator's qualified capability.	□ Pass □ Review □ N/A	
13. Release Verification	Confirm package data, stackup, via strategy, routing constraints and manufacturing requirements belong to the same approved release.	□ Pass □ Review □ N/A	

Important: This checklist does not define universal BGA pitch-to-via mappings, trace dimensions, via sizes or layer counts. Fanout strategy should be confirmed against the package geometry, PCB stackup, routing constraints, assembly requirements and selected fabricator capability.